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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,020	04/27/2005	Carl Glasse	1217/207	1660

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EXAMINER	
TAYLOR, EARL N	
ART UNIT	PAPER NUMBER
2818	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,020	GLASSE ET AL.	
	Examiner	Art Unit	
	EARL N. TAYLOR	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-13,15-17 and 20-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-13,15-17 and 20-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/26/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

The indicated allowability of previous claims 14, 16, 17 and 20-27 is withdrawn in view of the newly discovered reference(s) to Fukuda (U.S. Patent 6,096,585) submitted on applicant's IDS dated 26 February 2009. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9-13, 15-17 and 20-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Fukuda et al. (U.S. Patent 6,096,585).

Referring to Claim 13, Fukuda teaches in Fig. 2, for example, a method of fabricating a polycrystalline silicon channel (2a) TFT with a gate (4) overlying the channel (2a), having an upstanding gate (4) side wall, the method comprising the steps of:

(a) providing a gate (4) separated from a polycrystalline silicon layer (2) by an insulating layer (3);

(b) implanting a dopant (ion doping; Fig. 2b) into the polycrystalline silicon layer (2) using the gate (4) as a mask;

(c) forming a spacer (5) after step (b) adjacent to the gate (4) that comprises a conductive region which overlies the polycrystalline silicon layer (2) and extends along the gate (4) side wall, comprising depositing a layer of conductive material (titanium Fig. 2c) over the polycrystalline silicon layer (2) and the gate (4), and selectively etching the deposited layer of conductive material (titanium) to form the spacer (5) with a first portion overlying the polycrystalline silicon layer (2) and second portion extending along on the side wall of the gate (4), wherein the selective etching of the conductive layer (titanium) is carried out by forming a fillet (6) over the first portion thereof, and selectively etching the conductive layer (titanium) where not protected by the fillet (6), and wherein the fillet (6) is formed by depositing a further layer (SiOx; Fig. 2c) on said conductive layer (titanium), and selectively etching the further layer (SiOx) to form the fillet (6) therefrom and

(d) implanting a dopant (ion doping; Fig. 2e) into the polycrystalline silicon layer (2) using the gate (4) and the spacer (5) as a mask to form a source or drain region (2c), such that the spacer (5) overlies an LDD region (2b) in the polycrystalline silicon layer (2) between the source or drain region (2c) and the channel (2a).

Referring to Claim 9, Fukuda further teaches depositing the layer of conductive material (titanium) to a thickness which is less than that of the gate (4).

Referring to Claims 10-12, Fukuda further teaches depositing the layer of conductive material (titanium) as a metallic non-conformal layer by sputtering.

Referring to Claim 15, Fukuda teaches depositing the further layer (SiOx) as a conformal layer by PECVD.

Referring to Claim 28, Fukuda further teaches comprising the step of forming additional layers (7 and 9) over the fillet (6) after step (d).

Referring to Claim 29, Fukuda further teaches wherein the fillet (6) is retained over the spacer (5) after step (d), so that the fillet (6) remains within the TFT subsequently formed.

Referring to Claim 30, Fukuda further teaches wherein the fillet (6) remains over the spacer (5) after step (d) and within the TFT subsequently formed.

Referring to Claim 16, Fukuda teaches in Fig. 2, for example, a method of fabricating a polycrystalline silicon channel (2a) TFT with a gate (4) overlying the channel (2a), having an upstanding gate (4) side wall, the method comprising the steps of:

(a) providing a gate (4) separated from a polycrystalline silicon layer (2) by an insulating layer (3);

(b) implanting a dopant (ion doping; Fig. 2b) into the polycrystalline silicon layer (2) using the gate (4) as a mask;

(c) forming a spacer (5) after step (b) adjacent to the gate (4) that comprises a conductive region which overlies the polycrystalline silicon layer (2) and extends along the gate (4) side wall, comprising depositing a layer of conductive material (titanium) over the polycrystalline silicon layer (2) and the gate (4), and selectively etching the

deposited layer of conductive material (titanium) to form the spacer (5) with a first portion overlying the polycrystalline silicon layer (2) and a second portion extending along on the side wall of the gate (4), wherein the selective etching of the conductive layer is carried out by forming a fillet (6) over the first portion thereof, and selectively etching the conductive layer (titanium) where not protected by the fillet (6), wherein the fillet (6) is formed by depositing the a further layer (SiOx; Fig. 2c) as a Si containing layer on said conductive layer (titanium), and selectively etching the further layer (SiOx) to form the fillet (6) therefrom; and

(d) implanting a dopant (ion doping; Fig. 2e) into the polycrystalline silicon layer (2) using the gate (4) and the spacer (5), as a mask to form a source or drain region (2c), such that the spacer (5) overlies an LDD region (2a) in the polycrystalline silicon layer (2) between the source or drain region (2c) and the channel (2a).

Referring to Claim 20, Fukuda teaches depositing the layer of conductive material (titanium) to a thickness which is less than that of the gate (4).

Referring to Claims 21 and 22, Fukuda further teaches depositing the layer of conductive material (titanium) as a non-conformal layer by sputtering.

Referring to Claim 23, Fukuda teaches depositing the further layer (SiOx) as a conformal layer by PECVD.

Referring to Claim 17, Fukuda teaches in Fig. 2, for example, a method of fabricating a polycrystalline silicon channel (2a) TFT with a gate (4) overlying the

channel (2a), having an upstanding gate (4) side wall, the method comprising the steps of:

(a) providing a gate (4) separated from a polycrystalline silicon layer (2) by an insulating layer (3);

(b) implanting a dopant (ion doping; Fig. 2b) into the polycrystalline silicon layer (2) using the gate (4) as a mask;

(c) forming a spacer (5) after step (b) adjacent to the gate (4) that comprises a conductive region which overlies the polycrystalline silicon layer (2) and extends along the gate (4) side wall, comprising depositing a layer of conductive material (titanium) over the polycrystalline silicon layer (2) and the gate (4), and selectively etching the deposited layer of conductive material (titanium) to form the spacer (5) with a first portion overlying the polycrystalline silicon layer (2) and a second portion extending along on the side wall of the gate (4), wherein the selective etching of the conductive layer (titanium) is carried out by forming a fillet (6) over the first portion thereof, and selectively etching the conductive layer (titanium) where not protected by the fillet (6) wherein the fillet (6) is formed by depositing the a further layer (SiOx) by CVD on said conductive layer (titanium, and selectively etching the further layer (SiOx) to form the fillet (6) therefrom; and

(d) implanting a dopant (ion doping; Fig. 2e) into the polycrystalline silicon layer (2) using the gate (4) and the spacer (5) as a mask to form a source or drain region (2c), such that the spacer (5) overlies an LDD region (2b) in the polycrystalline silicon layer (2) between the source or drain region (2c) and the channel (2a).

Referring to Claim 24, Fukuda further teaches depositing the layer of conductive material (titanium) to a thickness which is less than that of the gate (4).

Referring to Claims 25 and 26, Fukuda further teaches depositing the layer of conductive material (titanium) as a non-conformal layer by sputtering.

Referring to Claim 27, Fukuda teaches depositing the further layer (SiOx) as a conformal layer by PECVD.

Conclusion

Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 26 February 2009 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Telephone / Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl N. Taylor whose telephone number is (571) 272-8894. The examiner can normally be reached on Monday-Friday from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Earl N. Taylor

/DAVID VU/
Primary Examiner, Art Unit 2818